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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/411,434	10/01/1999	JEAN-LOUIS TARDIEUX	TI-28234	8297

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EXAMINER
DECKTER, STEPHANIE M

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

14-G

Office Action Summary	Application No.	Applicant(s)	
	09/411,434	TARDIEUX, JEAN-LOUIS	
	Examiner	Art Unit	
	Stephanie M. Deckter	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on three applications filed in Europe on 03/08/99 and 10/06/98. It is noted, however, that applicant has not filed a certified copy of any of these European applications as required by 35 U.S.C. 119(b).

Information Disclosure Statement

2. The information disclosure statement filed 10/01/99 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. Applicant has not provided United States serial numbers for co-related cases labeled CA-CY. These references have not been considered. Please provide a table noting U.S. serial numbers and their corresponding docket numbers as provided on the original statement.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature. For example, please correct the phrase "There is, therefore, is a need" to --There is, therefore, a need to-- on page 3, line 8; please insert the word "of" in between the words "output" and "the" on line 12 of page 4; please replace the phrase "register of a part" with --register or a part-- in the 7th line of page 20; please replace the word "stall" with --stalls-- on page 26, line 17; please insert a period

after "(worst one)" on page 20, line 19 to denote the end of the sentence; please remove the word "the" on the 3rd line of page 27

5. The attempt to incorporate subject matter into this application by reference to "co-assigned application Serial No. _____ (TI-28433)" as listed on page 11, line 13, is improper because a U.S. serial number for this co-pending application. Applicant is required to provide the corresponding U.S. serial number.

6. The disclosure is objected to because of the following informalities: On line 6 of page 34, the referenced element number "Mux 2220" is incorrect as 2220 refers to the shadow [I] register. Please correct this number to refer to the appropriate element within figure 22. Also please correct the phrase "Figure 17" to read -- Figure 31 -- on page 40, lines 23 and 24.

Appropriate correction is required.

Drawings

7. Applicant is required to submit a proposed drawing correction in reply to all defects noted on the Notice of Draftperson's Patent Drawing Review (PTO-948). The objection to the drawings will not be held in abeyance.

8. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 303, 305, 307, 309, 311, and 313 as listed on page 18, line12; 823, 825, 827 as listed on line 20 of page 29; 2612 as listed on page 37, line 5; and 11 as listed on page 40, line 25. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

9. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 1420, 1444, 1450, 1451, 1460, 1461, 1462 are present in figure 14, but not mentioned in the discussion thereof within the specification on pages 26 and 27; 830, 832, 834, 836, and 875 of figure 16 which are further not mentioned in the discussion of this figure in the specification on pages 28 and 29; 1460, 1461, 1451, 1720a, and 1721 of figure 17; 2204 and 2208 of figure 22; 2514 of figure 25A; 2528 of figure 25B; 2629 and 2631 of figure 26B; 852, 854, 856, 858, and 889 of figure 27; and 15 of figure 31. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

10. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "2012" of figures 20 and 21 has been used to designate both the length register and Sh[I]2Reg Signals. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

11. Claims 4 and 10 recite the limitation "stall control signals output from the interlock circuitry" in the 3rd and 4th lines of the claims. There is insufficient antecedent basis for this limitation in the claim. The interlock circuitry only outputs a signal "controllably connected to the set of shadow registers" as set forth in claims 1 and 2, which further makes this claim unclear. It appears that the "stall control signals" being referred to are the ultimate merged stall signals as produced by the fourth level merge (1440) as discussed on page 29 of the specification

with reference to figures 14 and 16. Therefore, for the purposes of Examiner's prior art search, it is hereby assumed that the claim means "stall control signals output by the interlock circuitry based upon a result of arbitration between resources." Appropriate correction is required.

12. Claims 1-3, 6-9, 11, and 14 recite the limitation "protected resource" or "protected resources" in the 6th and 7th lines of claim 1, 4th line of claim 2, 2nd line of claim 3, 5th line of claim 6, 3rd line of claim 7, 2nd and 3rd line of claim 8, 4th line of claim 9, 3rd line of claim 11, and 4th and 5th line of claim 14. There is insufficient antecedent basis for this limitation in the claim as only a "plurality of resources," not specifically a plurality of **protected** resources is set forth in claim 1. Appropriate correction is required.

13. Claim 14 recites the limitation "selected shadow register" in the 6th and 7th lines of the claims. There is insufficient antecedent basis for this limitation in the claim as there is neither mention of a shadow register, nor a selected one thereof, prior to this limitation in the claim. Appropriate correction is required.

14. Claim 9 recites the limitation "wherein the stall vector filter" in the 1st and 2nd lines of the claim. There is insufficient antecedent basis for this limitation in the claim. Please correct claim 9 to read as claim 6 and introduce the limitation of the stall vector filter. Appropriate correction is required.

15. Claims 6 and 9 are objected to because of the following informalities: Please correct the 4th and 3rd line, respectively, of the claims from "that the each of select filter stages" to read -- that each of the select filter stages -- such that the word "the" is in the proper position. Appropriate correction is required.

16. Claim 14 is objected to because of the following informalities: Please delete the extraneous "the" between the words "for" and "each" in the 5th line of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

18. Claims 1, 2, 4, 5, 7, 14, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Smith and Sohi, "The Microarchitecture of Superscalar Processors," IEEE, 1995 (herein referred to as Smith). Referring to claim 1, Smith has taught a digital system having a processor comprising a processor pipeline with a plurality of pipeline stages (Smith page 1609, section A. Historical Perspective, first paragraph), a plurality of resources (Smith page 1610, section C. Elements of High Performance Processing, second paragraph) and a pipeline protection mechanism (Smith page 1614, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph), wherein the pipeline protection mechanism comprises:

a. a set of shadow registers (Smith page 1615, third full paragraph);

b. interlock circuitry for anticipating access conflicts for each protected resource between the pipeline stages (Smith page 1612, last paragraph in first column, continued in second column, first full paragraph in second column, and figure 2, as well as pages 1614-1615, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph) an

output of the interlock detection circuitry controllably connected to the set of shadow registers (Smith page 1615, third paragraph, particularly lines 5-13)

c. the set of shadow registers being interconnected with the processor such that a data item from a first pipeline stage can be redirected into a selected shadow register in response to an access conflict anticipated by the interlock circuitry so that a resource access conflict is resolved without stalling the processor pipeline (Smith page 1615, full paragraphs 1, 2, and 3).

19. Referring to claim 2, Smith has taught the interlock circuitry comprises:

a. interlock detection circuitry operable to anticipate access conflicts for all of the protected resources and operable to form a stall vector signal (Smith, pages 1614-1615, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph and page 1615, third full paragraph, first column, last sentence);

b. reservation and stall vector filtering circuitry connected to receive the stall vector signal and operable to select an available shadow register from the set of shadow registers in response to the stall vector signal (Smith, pages 1615, first column, third full paragraph starting at fifth line); and

c. shadow management circuitry connected to the reservation and filtering circuitry, the shadow management circuitry having an output signal controllably connected to the set of shadow registers (Smith page 1615, last full paragraph of first column and continued into second column, first full paragraph of second column, and figure 5).

20. Referring to claim 4, Smith has taught pipeline control logic for controlling the stages of the pipeline, the pipeline control logic being connected to receive stall control signals output

from the interlock circuitry based on the result of an arbitration between resources (Smith page 1615, third full paragraph, first column).

21. Referring to claim 5, Smith has taught at least one resource is selected from a group consisting of: a group of registers; a register; a field of a register; and a sub-field of a register (Smith page 1614, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph).

22. Referring to claim 7, Smith has taught the set of shadow registers is interconnected with the processor pipeline with multiplexing circuitry operable to redirect a read from a protected resource to a selected shadow register (Smith page 1615, second column, lines 7-10).

23. Referring to claim 14, Smith has taught a method of protecting a pipeline in a processor engine, wherein the processor includes a processor pipeline with a plurality of pipeline stages (Smith page 1609, section A. Historical Perspective, first paragraph) and a plurality of resources (Smith page 1610, section C. Elements of High Performance Processing, second paragraph), the method comprising the steps of:

a. separately arbitrating, for respective protected resources, to anticipate access conflicts between the pipeline stages for each resource (Smith page 1612, last paragraph in first column, continued in second column, first full paragraph in second column, and figure 2, as well as pages 1614-1615, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph), and

b. redirecting a data item from a first pipeline stage into a selected shadow register in response to an anticipated access conflict so that a resource access conflict is resolved without stalling the processor pipeline (Smith page 1615, full paragraphs 1, 2, and 3).

24. Referring to claim 15, Smith has taught the method further comprising the step of selectively stalling stages of the pipeline depending upon the result of the arbitration for the respective resources to avoid resource access conflicts if a shadow register is not available to resolve an anticipated access conflict (Smith page 1615, first column, third full paragraph).

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 3, 8, and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith and Sohi, "The Microarchitecture of Superscalar Processors," IEEE, 1995 (herein referred to as Smith) in view of Nelson et al., Digital Logic Circuit Analysis & Design, 1995 (herein referred to as Nelson). Referring to claims 3 and 8, Smith has taught interlock circuitry comprises arbitration circuitry for each protected resource (Smith page 1612, last paragraph in first column, continued in second column, first full paragraph in second column, and figure 2, as well as pages 1614-1615, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph). Smith has not taught each arbitration circuit definable as a specific form of a single, generic arbitration function. Nelson has taught the use of a generic logic function to create smaller, more specific forms of such logic (Nelson pages 173-187), such that each resource only requires enough logic to determine if there will be contention for that particular register. This would have allowed minimal use of logic as opposed to utilizing all possible logic to determine if any resource conflict has occurred (Nelson page 173, second paragraph). Therefore, it would

have been obvious to a person of ordinary skill in the art at the time the invention was made to use the method of Nelson to create each arbitration logic as a specific form of a single, generic arbitration function.

27. Referring to claim 9, Smith has not explicitly taught the interlock circuitry comprising a stall vector filter, wherein the stall vector filter has a plurality of select filter stages connected in a serial manner such that each of the select filter stages is associated with a corresponding protected resource. Smith has taught a mapping table that associates a physical register with the current value of a logical register (Smith page 1615, third full paragraph, lines 3-5). Instead of maintaining a mapping table to do such, an easier method would have been to include various filter stages associated with each resource that defined the register rename information for that particular resource. Furthermore, it would have been beneficial to serially connect each filter stage in order to communicate the register rename information to other resources and thus, other stages of the pipeline. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to connect a plurality of select filter stages in a serial manner and associate one stage with each protected resource.

28. Referring to claim 10, Smith has taught pipeline control logic for controlling the stages of the pipeline, the pipeline control logic being connected to receive stall control signals output from the interlock circuitry based on the result of an arbitration between resources (Smith page 1615, third full paragraph, first column).

29. Referring to claim 11, Smith has taught the set of shadow registers is interconnected with the processor pipeline with multiplexing circuitry operable to redirect a read from a protected resource to a selected shadow register (Smith page 1615, second column, lines 7-10).

30. Referring to claim 12, Smith has taught at least one resource is selected from a group consisting of: a group of registers; a register; a field of a register; and a sub-field of a register (Smith page 1614, section B. Instruction Decoding, Renaming, and Dispatch, first paragraph).

31. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith and Sohi, "The Microarchitecture of Superscalar Processors," IEEE, 1995 (herein referred to as Smith). Smith has not explicitly taught the interlock circuitry comprising a stall vector filter, wherein the stall vector filter has a plurality of select filter stages connected in a serial manner such that each of the select filter stages is associated with a corresponding protected resource. Smith has taught a mapping table that associates a physical register with the current value of a logical register (Smith page 1615, third full paragraph, lines 3-5). Instead of maintaining a mapping table to do such, an easier method would have been to include various filter stages associated with each resource that defined the register rename information for that particular resource. Furthermore, it would have been beneficial to serially connect each filter stage in order to communicate the register rename information to other resources and thus, other stages of the pipeline. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to connect a plurality of select filter stages in a serial manner and associate one stage with each protected resource.

32. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith and Sohi, "The Microarchitecture of Superscalar Processors," IEEE, 1995 (herein referred to as Smith) in view of Burke et al., U.S. Patent Number 5,333,176 (herein referred to as Burke). Smith has taught each of the limitations of claim 1 from which claim 13 depends. However, Smith has not taught the digital system being a cellular telephone, further comprising an integrated keyboard

connected to the processor via a keyboard adapter; a display, connected to the processor via a display adapter; radio frequency (RF) circuitry connected to the processor; nor an aerial connected to the RF circuitry. Burke has taught a the digital system being a cellular telephone, further comprising an integrated keyboard connected to the processor via a keyboard adapter (figure 1, element 11 and figure 3, element 130); a display, connected to the processor via a display adapter (figure 1, element 12 and figure 3, 124)); radio frequency (RF) circuitry connected to the processor (column 5, lines 6-14 and figure 6); and an aerial connected to the RF circuitry (figure 1). It is advantageous to use digital processors requiring low power consumption in cellular telephones in order to allow the phones to run on only a small battery for as long as possible. Processors that are fast and employ instruction-level parallelism consume less power than slower, non-Superscalar processors. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to replace the processor within the cellular telephone of Burke with the fast, Superscalar microprocessor of Smith in order to reduce power consumption.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Staplin et al., U.S. Patent Number 5,073,855, have taught a pipeline protection mechanism that utilizes separate arbitration logic for each protected resource to detect conflicts between pipeline stages.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephanie M. Deckter whose telephone number is 703-308-6132. The examiner can normally be reached on 8:00 A.M. - 5:30 P.M. with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Stephanie M. Deckter
Examiner
Art Unit 2183

SMD

smd
March 4, 2002

EDDIE CHAN
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